REMARKS

With regard to the rejection of independent claim 80, and thus its dependent claims, under 35 U.S.C. §112, second paragraph, amendments are being made to claim 80 to correct the lack of antecedent basis for the designated limitations, without affecting the scope of these claims. It is appreciated that the Examiner pointed out these errors. Also, two minor changes are being made to independent claim 71 to make its terminology consistent.

Prior Art Rejections of Independent Claims 63, 71 and 80

All three of the independent claims 63, 71 and 80 in this application have been rejected under 35 U.S.C. §103 over a combination of U.S. patents nos. 4,757,474 ("Fukushi et al."), 4,949,309 ("Rao") and 4,466,059 ("Bastian et al."), plus "common practices in the art" of which Official Notice has been taken. Reconsideration of this ground of rejection is respectfully requested.

Three plus references have been cited in support of the obviousness rejection of the rather specific independent claims in the present application. Fukushi et al. has been cited for its use of a redundant memory portion in a volatile memory system that is substituted for a main memory portion. Rao has been cited for erasing blocks of cells in a non-volatile memory. Bastian has been cited for movement of data into and out of a cache memory that is provided as part of a magnetic disk memory system. Official Notice has additionally been taken (Office Action, p. 5, para. vi.) of several items of specific knowledge that one of ordinary skill would allegedly have employed to combine the teachings of these three patent references along the lines of the claims.

The independent claims in issue each define either a method of operation of a non-volatile memory system, or the memory system itself, with specific interactions specified between the cache memory and the non-volatile memory to store data in blocks either directly mapped from the host address or remapped to avoid unusable blocks. Nothing close to these specific interactions has been found to be suggested by the three cited patent references themselves. Each of the references is directed to a narrow aspect of the operation of different memory technologies, as briefly summarized in the preceding paragraph. As such, the references do not provide evidence of motivation to

combine their teachings in the manner claimed. The only evidence stated in the Office Action of a motivation to combine the teachings of these references are several "facts" of which Official Notice has been taken (Office Action, p. 5, para. vi). It is respectfully submitted that the Office Action discussion of what one ordinarily skilled in the art would have done with the teachings of the prior art is highly speculative, and based upon a hindsight analysis.

An objection is separately made to the taking of Official Notice of the motivational factors. If the rejection is maintained, citation of prior art references or other evidence to establish the assumed facts is requested. It is difficult to respond to a rejection that assumes one skilled in the art knows so many specific items of information without being able to consider references being relied upon for a description of such information. It is respectfully submitted, absent citation of such references, that a *prima facie* case of obviousness has not been made.

Dependent Claims 64 – 70, 72 – 79, and 81 – 89

All of the pending dependent claims have been rejected as obvious over the Fukushi et al., Rao and Bastian patent references, as above, plus items of which Official Notice has been taken. Therefore, these dependent claims are believed to be patentable over the cited prior art for the same reasons as expressed above with respect to their parent independent claims 63, 71 and 80. The rejections of claims 75 and 84 are based upon a combination of references including an additional patent, for a total of four patent references being relied upon.

Objection is also made to the rejections based on additional prior art of which Official Notice has been taken. At least some prior art appears to have been assumed to exist with respect to nearly every one of the dependent claims.

Double Patenting Rejection

Certain claims have been rejected on obviousness double patenting grounds. U.S. patent no. 5,764,888 is first mentioned (Office Action, p. 7) but the specifics then refer to U.S. patent No. 5,297,148. However, the '888 patent is not commonly assigned with the present application and is otherwise totally unrelated. And the '148 patent, although

commonly assigned with the present application, contains only claims 1 – 4 while the rejection refers to claims 44 and 45. Therefore, a response to this ground of rejection as expressed cannot be made.

This inability to respond has been discussed with Examiner Hua by telephone, who, since he was unable to locate the Patent and Trademark Office file of the present application at the time, suggested that the above explanation be given in response to this ground of rejection.

Information Disclosure Statement

The Examiner's consideration and making of record the many references listed in two Information Disclosure Statements previously filed in this application is appreciated. However, three "Other Documents" listed on one PTO form 1449 page omit the Examiner's initials. Therefore, a copy of this page is attached hereto. It is respectfully requested that the Examiner indicate the consideration of these three references by initialing those items on the attached page and making the page part of record in the file of the present application.

Conclusion

An early indication of the allowance of the present application is solicited. However, if the Examiner wants to clarify the double patenting rejection or has any further issues that need to be considered, he is invited to telephone the undersigned attorney at 415-217-6293.

EXPRESS MAIL LABEL NO:

EL873331098US

Respectfully submitted,

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AMENDED CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

71. (Amended) A method of a host system utilizing a mass data storage system to store data files, said mass data storage system including an array of non-volatile EEprom memory cells partitioned into a plurality of blocks that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

writing individual new data files from the host to a cache memory provided as part of the mass data storage system without writing the new data files to the memory cell array,

when written into the cache memory, reading a data file requested by the host system from the cache memory rather than from the memory cell array,

thereafter writing a selected data file from the cache memory into the memory cell array, said writing including selecting at least one usable memory cell block into which the data file is written that includes either (a) the memory cell block whose address is mapped from a mass storage system address received from the host system, or (b) if the memory cell block whose address is mapped from the received mass storage system address is not ~~useful~~usable, another memory cell block that is ~~useful~~usable,

when written into the memory cell array, reading a data file requested by the host system from the memory cell array rather than from the cache memory.

80. (Amended) A bulk storage memory system that is connectable to a host system, said memory system comprising:

an array of non-volatile memory cells arranged to store in designated blocks thereof a given amount of user data and associated overhead data,

a cache memory separate from said non-volatile memory cell array, and

a controller connectable to said host system for controlling operation of the non-volatile memory cell array and the cache memory, said controller including:

an erasing circuit that causes all of the memory cells of one or more designated blocks of the array to be erased together,

an addressing circuit responsive to receipt of a mass memory storage block address from the host system to generate an address of at least one

corresponding array block, the addressing circuit being responsive to a list of array blocks that have other array blocks substituted therefore to substitute at least one address of such other array blocks for the generated address of said at least one array block,

a first data transfer circuit responsive to the addressing circuit to execute an instruction from the host system to perform a designated one of (1) a data write operation by writing user data to the cache memory, or (2) a data read operation by reading addressed user data first from the cache memory, if stored therein, or from the array, if not stored in the cache memory, and

a second data transfer circuit that removes data from the cache by writing ~~said removed~~ the data so removed into the ~~memory~~ array of non-volatile memory cells.

TEXT OF ALL APPLICATION CLAIMS AFTER AMENDMENT

1 ~~63.~~ A method of operating a memory that includes an array of non-volatile EEprom memory cells partitioned into a plurality of blocks that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

maintaining a link between addresses of any unusable memory cell blocks and addresses of substitute usable memory cell blocks,

in response to a write request from a host system, initially writing new data intended for the EEprom memory cell array into a cache memory instead of the EEprom memory cell array,

thereafter, in response to additional space for new data being required in the cache memory, directing at least a portion of the data stored in the cache memory to be written into the EEprom memory cell array with an address including at least one of said memory cell blocks, and

writing said at least a portion of the data stored in the cache memory into the EEprom memory cell array by a method including:

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if said at least one of said memory cell blocks is usable, writing said at least a portion of the data stored in the cache memory into said at least one of said memory cell blocks, and

if said at least one of said memory cell blocks is unusable, writing said at least a portion of the data stored in the cache memory into at least one of the substitute usable memory cell blocks that is linked with said at least one of said memory cell blocks.

2 1
~~64.~~ The method of claim ~~63,~~ wherein said at least a portion of the data stored in the cache memory that is written into the EEprom memory cell array includes that which has been stored in the cache memory for the longest time.

3 1
~~65.~~ The method of claim ~~63~~, wherein the individual blocks of memory cells are operated with both user data and overhead data stored therein in non-overlapping portions of the individual blocks.

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4 3
~~66.~~ The method of claim ~~65~~, wherein overhead data stored in the individual blocks of memory include a characteristic of the individual block in which the user data and overhead data are stored.

5 3
~~67.~~ The method of claim ~~65~~, wherein overhead data stored in the individual blocks of memory includes an error correction code for the user data stored in the same blocks.

6 3
~~68.~~ The method of claim ~~65~~, wherein overhead data stored in the individual blocks of memory include an address corresponding to the block in which the overhead data are stored.

7 1
~~69.~~ The method of claim ~~63~~, wherein writing at least a portion of the data stored in the cache memory into the EEprom memory cell array includes programming individual memory cells of the EEprom memory cell array into exactly two states in order to store exactly one bit of data per cell.

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8 1
~~70.~~ The method of claim ~~63~~, wherein writing at least a portion of the data stored in the cache memory into the EEprom memory cell array includes programming individual memory cells of the flash EEprom system into more than two states in order to store more than one bit of data per cell.

9
~~71.~~ (Amended) A method of a host system utilizing a mass data storage system to store data files, said mass data storage system including an array of non-volatile EEprom memory cells partitioned into a plurality of blocks that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

writing individual new data files from the host to a cache memory provided as part of the mass data storage system without writing the new data files to the memory cell array,

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when written into the cache memory, reading a data file requested by the host system from the cache memory rather than from the memory cell array,

thereafter writing a selected data file from the cache memory into the memory cell array, said writing including selecting at least one usable memory cell block into which the data file is written that includes either (a) the memory cell block whose address is mapped from a mass storage system address received from the host system, or (b) if the memory cell block whose address is mapped from the received mass storage system address is not usable, another memory cell block that is usable,

when written into the memory cell array, reading a data file requested by the host system from the memory cell array rather than from the cache memory.

10 9
~~72.~~ The method of claim ~~71~~, wherein the individual new data files are written into a volatile random-access-memory as the cache memory.

11 9
~~73.~~ The method of claim ~~71~~, wherein the individual new data files are written into a memory separate from the flash EEprom system as the cache memory.

12 9
~~74.~~ The method of claim ~~71~~, wherein the mass data storage system is provided on a card that is electrically and mechanically removably connectable with the host computing system.

13 12
~~75.~~ The method of claim ~~74~~, wherein the mass data storage system provides an ATA interface with the host computing system.

14 9
~~76.~~ The method of claim ~~71~~, wherein selecting a data file and writing the selected data file to the EEprom memory cell array is caused to occur when additional space for new data files is required in the cache memory.

15 9
~~77.~~ The method of claim ~~71~~, wherein the data file selected to be written into the memory cell array is selected based upon a length of time since the data file was last written into the cache memory.

16

~~78.~~ The method of claim 9 ~~71~~, wherein writing a new data file to the cache memory from the host occurs in less time than if written directly into the EEprom memory cell array from the host.

17

~~79.~~ The method of claim 9 ~~71~~, wherein the individual blocks of memory cells are operated with both user data and overhead data stored therein in non-overlapping portions of the individual blocks.

18

~~80.~~ (Amended) A bulk storage memory system that is connectable to a host system, said memory system comprising:

an array of non-volatile memory cells arranged to store in designated blocks thereof a given amount of user data and associated overhead data,

a cache memory separate from said non-volatile memory cell array, and

a controller connectable to said host system for controlling operation of the non-volatile memory cell array and the cache memory, said controller including:

an erasing circuit that causes all of the memory cells of one or more designated blocks of the array to be erased together,

an addressing circuit responsive to receipt of a mass memory storage block address from the host system to generate an address of at least one corresponding array block, the addressing circuit being responsive to a list of array blocks that have other array blocks substituted therefore to substitute at least one address of such other array blocks for the generated address of said at least one array block,

a first data transfer circuit responsive to the addressing circuit to execute an instruction from the host system to perform a designated one of (1) a data write operation by writing user data to the cache memory, or (2) a data read operation by reading addressed user data first from the cache memory, if stored therein, or from the array, if not stored in the cache memory, and

a second data transfer circuit that removes data from the cache by writing the data so removed into the array of non-volatile memory cells.

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~~81.~~ The memory system according to claim 18 ~~80~~, wherein the second data transfer circuit removes data from the cache in response to additional space for new data being required in the cache memory.

20
~~82.~~ The memory system according to claim 18 ~~80~~, wherein the second data transfer circuit removes data from the cache that has been stored in the cache memory for a time longer than the remaining data therein.

21
~~83.~~ The memory system according to claim 18 ~~80~~, wherein the list of array blocks that have other array blocks substituted therefore includes inoperable or defective blocks.

22
~~84.~~ The memory system according to claim 21 ~~83~~, wherein the inoperable or defective blocks include blocks that contain a number of defective cells in excess of a preset number.

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23
~~85.~~ The memory system according to claim 18 ~~80~~, wherein said given amount of user data is 512 bytes.

24
~~86.~~ The memory system according to claim 18 ~~80~~, wherein said bulk storage memory system is implemented in a single package that is removably connectable to the host system through an electrical connector.

25
~~87.~~ The memory system according to claim 18 ~~80~~, wherein the overhead data stored in an individual one of the memory cell array blocks includes an error correction code of the user data stored in said individual block.

26
~~88.~~ The memory system according to claim 18 ~~80~~, wherein the first and second data transfer circuits write data into the memory cell array with exactly two

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programmable states per memory cell storage element, thereby to store exactly one bit of data per storage element.

27 18
~~89.~~ The memory system according to claim ~~80~~, wherein the first and second data transfer circuits write data into the memory cell array with more than two programmable states per memory cell storage element, thereby to store more than one bit of data per storage element.

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